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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,470	MUKUND ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
12/11/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 21 September 2006. These drawings are acceptable

Withdrawn Objections

2. Applicant, via amendment has overcome the objection of claims 13-20. The objection has been respectfully withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Narayan et al. (U.S. Patent No. 5,822,559), herein referred to as Narayan et al.'559.

Referring to claim 1, Narayan et al.'559 discloses, as claimed, a networking application processor (see Fig. 2), comprising: an input socket configured to receive data packets (the input data from I/O module of the system intended to be used); a memory (such as main memory of the Narayan et al.'559's system or instruction cache 204, see Fig. 2) for storing instructions; circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access an operand from a memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2); an arithmetic logic unit (ALU) (inside function units 212A-212D, see Fig. 2); and circuitry for aligning operands (such as instruction alignment unit 206 or decode units 207, see Fig. 2, and col. 6, lines 62-67) to be processed by the ALU, the circuitry for aligning operands causing the operand to be aligned by a lowest significant bit, wherein the circuitry for aligning the operand supplies an extension (in the situation when the real operand size is less than the size to be processed) to the operand to allow the ALU to process different size operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

Referring to claim 14, Narayan et al.'559 discloses, as claimed, a processor capable of processing a data packet associated with a processing stage of a pipeline of processors, the processor comprising: a data random access memory (RAM) (such as the main memory of the Narayan et al.'559's system) configured to enable access to

data structures; instruction fetch and decode circuitry (comprising such as early decode units 207A-207D, see Fig. 2) configured to interpret instructions to be executed by an arithmetic logic unit (ALU) (function units 212A-212D, see Fig. 2), the instruction fetch and decode circuitry including, a read only memory (ROM) (such as portion of the main memory of the Narayan et al.'559's system comprising system codes), the ROM configured to store code common to each processing stage associated with a pipeline of processors; a code RAM (MROM unit 209, see Fig. 2), the code RAM configured to download code specific to the processing stage; and instruction decode circuitry (comprising such as decode units 208A-208D, see Fig. 2) configured to recognize operating instructions; execute and write back circuitry (comprising function units 212A-212D, see Fig. 2) configured to set up operands to be processed by the ALU, the execute and write back circuitry including, internal registers (inside register file 218, see Fig. 2) for defining a first and a second operand; an arithmetic logic unit (function units 212A-212D, see Fig. 2) for processing the first and second operands; and align function circuitry (instruction alignment unit 206, see Fig. 2) for aligning the first and the second operands to be processed by the ALU, the align function circuitry causing the first and the second operands to be aligned by a lowest significant bit, wherein the align function circuitry supplies an extension (in the situation when the real operand size is less than the size to be processed) to the each of the operands to allow the ALU to transparently process different size operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

As to claim 2, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the instructions have a width of 96 bits (see the instruction set in Fig. 1 when it comprises 12 bytes=96 bits), and wherein the single cycle access enables the data to be addressed and operated on in a single cycle in a single clock cycle without being placed into a register (see col. 10, last paragraph).

Note that if an instruction is fetched, the data contained within that instruction is addressed (with a program counter) and operated on (read from memory). The definition of the word "operate" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "to perform a function; work". Under this definition, a read (fetch) from memory is reasonably considered to be an operation.

As to claims 3 and 16, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the different size operands are selected from the group consisting of 8 bit operands, 16 bit operands, and 32 bit operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits).

As to claim 4, Narayan et al.'559 also discloses: the networking application processor of claim 1, further including: an output socket for transmitting processed data; and a 64 bit bus (see such as 64-bit input bus to decode unit 0-3, see Fig. 25) connecting the input socket and the output socket.

As to claims 5 and 15, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the extension to the operand fills each higher bit with a value (such as 0 for each higher bit for the unsigned operands).

As to claim 6, Narayan et al.'559 also discloses: the networking application processor of claim 1, wherein the operand is selected from the group consisting of a source operand, a destination operand, an immediate operand, and an internal register

operand (see col. 2, lines 5-23, and Fig. 1, regarding the instruction set format including source operand, a destination operand, an immediate operand).

As to claim 17, Narayan et al.'559 also discloses: the processor of claim 14, wherein the operating instructions wherein the operating instructions are formatted as 96 bit instructions (see the instruction set 100 in Fig. 1 when it comprises 12 bytes=96 bits), each of the 96 bit instructions including a single return bit (the bit such as end of file or record in the instruction set 100 in Fig. 1).

As to claim 18, Narayan et al.'559 also discloses: the processor of claim 14, wherein the processor is configured as a two stage pipeline for pipelining an instruction fetch and decode operation (using prefetch/predecode unit 202; and decode units 208A-208D, see Fig. 2) and an execute and write back operation (see Col. 144, lines 45-65, regarding write back operations).

As to claim 19, Narayan et al.'559 also discloses: the processor of claim 14, wherein the operating instructions include microcode configured to predict a likely direction for a branch instruction (using branch prediction unit 220, see Fig. 2).

As to claim 20, Narayan et al.'559 also discloses: the processor of claim 19, wherein no operation (NOP's) instructions are included (see such as col. 139, lines 4-5, regarding some of the instructions may be NOOP), the NOP's configured block an invalidated pre-fetched instruction.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayan et al.'559.

Referring to claim 7, Narayan et al.'559 discloses, as claimed, a processor (see Fig. 2), comprising: an input socket (the input data from I/O module of the system intended to be used) configured to receive data packets; a memory (such as main memory of the Narayan et al.'559's system or instruction cache 204, see Fig. 2) for storing instructions; circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access from a memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2); and an arithmetic logic unit (ALU) (inside function units 212A-212D, see Fig. 2), the ALU configured to receive a first and a second operand (operand A and operand B, see Fig. 33); the second operand being specified from an internal register (REGF, see Fig. 33).

Narayan et al.'559 discloses the claimed invention except for explicitly showing the first operand having a mask enabling the ALU to process a non-masked segment of the first operand.

However, Narayan et al.'559 shows using masks to select bytes before sending to the register file for the further use (see Col. 144, lines 59-60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Narayan et al.'559's system to comprise the first operand having a mask enabling the ALU to process a non-masked segment of the first operand,

as also taught by Narayan et al.'559, in order to facilitate selecting the useful bytes to be processed and saving the processing time in the Narayan et al.'559's system.

As to claim 8, Narayan et al.'559 also discloses: the instructions have a width of 96 bits (see the instruction set in Fig. 1 when it comprises 12 bytes=96 bits) as set forth in claim 2 above.

As to claim 9, Narayan et al.'559 also discloses: the processor of claim 7, wherein each of the instructions include a loadback feature enables random accesses to one of a source indirect register or a destination indirect register through indirect addressing (see Fig. 1 and col. 2, lines 5-22 regarding such as adding the displacement value to the content of a register to form a memory location).

As to claim 10, Narayan et al.'559 also discloses: the processor of claim 7, wherein the mask is associated with an immediate value (see Fig. 1, the instruction set comprising the immediate field) of the first operand.

As to claim 11, Narayan et al.'559 also discloses: first and the second operands are associated with a size selected from the group consisting of 8 bit operands, 16 bit operands, and 32 bit operands (see col. 17, lines 32-42, regarding the operand size may be 8, 16, and 32 bits) as set forth in claim 3 above.

As to claim 12, Narayan et al.'559 also discloses: the processor of claim 7, wherein the first operand is selected from the group consisting of a source operand, a destination operand, an immediate operand, and an internal register operand (see col. 2, lines 5-23, and Fig. 1, regarding the instruction set format including source operand, a destination operand, an immediate operand) as set forth in claim 6 above.

As to claim 13, Narayan et al.'559 also discloses: the method of claim 7, wherein the memory location (such as main memory of the Narayan et al.'559's system or data cache 224, see Fig. 2) is a static random access memory (SRAM).

Response to Arguments

7. Applicant's arguments filed 21 September 2006 have been fully considered but they are not persuasive.

8. Applicant states:

> The Examiner asserts that Narayan discloses the feature of circuitry configured to access data structures associated with a processing stage, the circuitry configured to access data structures enabling a single cycle access of an operand from a memory location. In support of this assertion the Examiner refers to the main memory or the data cache of Figure 2. Applicants respectfully disagree with this assertion and submit that neither the Examiner nor Narayan specifies what the circuitry enables a single cycle access of an operand from memory. Applicants respectfully request that the Examiner specify where Narayan discloses any circuitry enabling a single cycle access, i.e., where the operand can be addressed and operated on in a single clock cycle (see the present application page 17, lines 21-23 for the definition of single cycle access, which is further specified in amended claim 2). If the Examiner is referring to memory or data cache 224 as having circuitry enabling a single cycle access, Applicants respectfully request that the Examiner specify where this feature is specified as nowhere in Narayan is this capability discussed. Furthermore, as stated in column 66, lines 22-25, an extra clock cycle is needed for decoding instructions having more than 4 prefix bytes. Even if there was only one clock cycle used to decode the prefix byte, because the operand still needs to be operated on.

Examiner disagrees. The specification makes no specific definition of the term "single cycle access". Page 17 of the present application merely states that an embodiment of the invention accesses memory in one clock cycle and performs a "single cycle access". The term cycle can be broadly interpreted as the time period required to perform an action. Therefore, a single cycle need not directly correlate with

the clock cycle and any read is performed within one read cycle. Further, fetching an instruction (which is data) from memory is done in one clock cycle (see above regarding claim 2).

9. Applicant states:

> The Examiner further states that the feature of circuitry for aligning operands to be processed by the ALU, the circuitry for aligning operands causing the operands to be aligned by a lowest significant bit, wherein the circuitry for aligning the operands supplies an extension to the operands to allow the ALU to process different size operands is taught in column 17, lines 32-42. Applicants respectfully request that the Examiner explain how a prefix designating the bit size of the operand discloses aligning operands by a lowest significant bit. First of all the prefix deals with a single operand and nowhere is it mentioned that multiple operands are aligned by a lowest significant bit. The decoding process referred to by the Examiner is for determining the size of the operand to determine where to route the operand and for complex instructions (see column 16). Furthermore, the Applicants would like for the examiner to explain how the prefixes for multiple operands would be aligned as nowhere is this mentioned is Narayan. Accordingly, claims 1-6 are allowable for at least these reasons.

Examiner disagrees. If any data is stored in a space larger than the data itself, it must be aligned in some fashion. The lowest significant bit must be aligned at some point in the physical register. This is considered to be aligning operands by a lowest significant bit. Further, it is unreasonable to say that there is only 1 operand used by the processor. While running a program, multiple operands will be aligned.

10. Applicant states:

> Claim 14 includes the features of a read only memory (ROM), the ROM configured to store code common to each processing stage associated with a pipeline of processors and a code RAM configured to download code specific to the processing stage and wherein the code specific to the processing stage is enabled for single cycle access. The Examiner never provides any analysis of where Narayan teaches a ROM configured to store code common to each processing stage associated with a pipeline of processors. Narayan does not have a pipeline of processors and is silent as to this feature. Applicants respectfully request that the Examiner address this feature or withdraw this rejection. The Examiner further asserts that the MROM unit of Narayan discloses the code RAM. As the

> MROM unit of Narayan breaks down complex instruction to simpler instruction, the Applicants submit that the MROM unit is a processor and not a memory unit (see column 3, lines 45-65, and column 6, lines 20-30).

Examiner disagrees. Narayan discloses the use of ROM for micro-operations related to the pipeline stages (see col. 22, lines 29-33). Further the MROM stores micro instructions to be executed by the pipeline.

11. Applicant states:

> In addition, as specified in claim 14, the code RAM and the ROM are part of the fetch and decode circuitry. The examiner is asserting that a portion of the main memory and the MROM unit is includes in the fetch and decode circuitry and refers to Figure 2 of Narayan. As illustrated in Figure 2, the MROM unit and the Main memory are different blocks and the main memory is not even in communication with the early decode units or the MROM. Applicants respectfully request that the Examiner specify what basis there is for classifying the MROM and a portion of the main memory as fetch and decode circuitry.

Examiner disagrees. The MROM and main memory are considered to be part of the fetch and decode circuitry because they assist with the fetch and decode process. The term "fetch and decode circuitry" is extremely broad, and anything related to fetching or decoding can reasonably be considered part.

12. Applicant states:

> In addition the Examiner asserts that the feature of an arithmetic logic unit (ALU), the ALU configured to receive a first and a second operand; the second operand being specified from an internal register, the first operand having a mask enabling the ALU to process a non-masked segment of the first operand. The Applicants respectfully disagree with this characterization. First of all, the Examiner states that the functional units of Figure 33 include the ALU, then the Examiner states that REGF is the internal register of the ALU. In Figure 33 REGF is external to the ALU. Applicants respectfully request that the Examiner specify the basis for modifying the external REGF to be internal to the ALU

> if this rejection is maintained in light of the minimal discussion of Figure 33 in the specification.

Examiner disagrees. Examiner considers both the functional units and the REGF to be the ALU. The term ALU merely requires that the unit perform arithmetic and/or logic operations. The register assists with these operations, and is therefore considered to be part of the ALU. No physical modification is needed for the REGF to be considered part of an ALU. The claim does not recite any specific limitations as to exclude this reasonable interpretation.

13. Applicant states:

> In addition the Examiner asserts that the feature of an arithmetic logic unit (ALU), the ALU configured to receive a first and a second operand; the second operand being specified from an internal register, the first operand having a mask enabling the ALU to process a non-masked segment of the first operand. The Applicants respectfully disagree with this characterization. First of all, the Examiner states that the functional units of Figure 33 include the ALU, then the Examiner states that REGF is the internal register of the ALU. In Figure 33 REGF is external to the ALU. Applicants respectfully request that the Examiner specify the basis for modifying the external REGF to be internal to the ALU if this rejection is maintained in light of the minimal discussion of Figure 33 in the specification.

Examiner disagrees. Examiner considers both the functional units and the REGF to be the ALU. The term ALU merely requires that the unit perform arithmetic and/or logic operations. The register assists with these operations, and is therefore considered to be part of the ALU. No physical modification is needed for the REGF to be considered part of an ALU. The claim does not recite any specific limitations as to exclude this reasonable interpretation.

14. Applicant states:

> The Examiner admits that Narayan does not teach the first operand having a mask. However, according to the Examiner, one skilled in the art would have looked to column 144 and saw a mask was applied to status bits that ensure that write back destinations are not the same, when the status bits are set for destinations of different size. Applicants disagree with this assertion as applying a mask to status bits for a write back interface provides motivation for applying a mask to one of two operands for processing by an ALU. As Narayan never discusses processing two operands at a time one skilled in the art would not have modified Narayan as suggested by the Examiner.

Examiner disagrees. The claim does not recite any limitations forcing a mask on **only** one register.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 12/11/2006

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